IN THE CLAIMS:

Please cancel claims 1-20 without prejudice or disclaimer as to the subject matter recited therein.

Please amend the claims as follows.

1-20. Cancelled.

21-25. Cancelled.

26. (New) A cache memory system comprising:

a cache controller; and

a cache memory coupled to said cache controller for storing a plurality of cache lines, wherein said cache memory includes a plurality of memory sections, wherein each of said memory sections is separately addressable through separate address lines coupled to said cache controller, and wherein each cache line includes an address tag and corresponding data;

wherein said cache controller is configured to store a portion of each of said plurality of cache lines in each of said plurality of memory sections, and wherein said cache controller is further configured to read a portion of a particular cache line concurrently with writing another portion of the particular cache line.

27. (New) The cache memory system as recited in claim 26, wherein said cache controller is configured to read the data of the particular cache line concurrently with writing the address tag of the particular cache line.

28. (New) The cache memory system as recited in claim 26, wherein said cache controller is further configured to concurrently access the address tag corresponding to a second cacheline and the address tag corresponding to a third cache line.

29. (New) The cache memory system as recited in claim 28, wherein said second cache line corresponds to a given snoop request and wherein said third cache line corresponds to another snoop request.

30. (New) The cache memory system as recited in claim 26, wherein each of said plurality of memory sections is provided on a separate memory chip.

31. (New) The cache memory system as recited in claim 26, wherein said address tag of each cache line is included in a tag field, and wherein said tag field further stores state information indicative of a coherency state of said corresponding data.

32. (New) The cache memory system as recited in claim 31, wherein each of said plurality of memory sections is provided on a separate memory chip.

33. (New) A computer system comprising:

a processor;

a cache controller coupled to the processor; and

a cache memory coupled to said cache controller for storing a plurality of cache lines, wherein said cache memory includes a plurality of memory sections, wherein each of said memory sections is separately addressable through separate address lines coupled to said cache controller, and wherein each cache line includes an address tag and corresponding data;

wherein said cache controller is configured to store a portion of each of said plurality of cache lines in each of said plurality of memory sections, and wherein said cache controller is further configured to read a portion of a particular cache line concurrently with writing another portion of the particular cache line.

34. (New) The computer system as recited in claim 33, wherein said cache controller is configured to read the data of the particular cache line concurrently with writing the address tag of the particular cache line.

35. (New) The computer system as recited in claim 33, wherein said cache controller is configured to concurrently access the first address tag corresponding to a second cache line and the address tag corresponding to a third cache line.

36. (New) The computer system as recited in claim 35, wherein said second cache line corresponds to a given snoop request and wherein said third cache line corresponds to another snoop request.

37. (New) The computer system as recited in claim 33, wherein each of said plurality of memory sections is provided on a separate memory chip.

38. (New) The computer system as recited in claim 33, wherein said address tag of each cache line is included in a tag field, and wherein said tag field further stores state information indicative of a coherency state of said corresponding data.

39. (New) A cache memory system comprising:

a cache controller; and

a cache memory coupled to said cache controller for storing a plurality of cache lines, wherein said cache memory includes a plurality of memory sections, wherein each of said memory sections is separately addressable through separate address lines coupled to said cache controller, and wherein each cache line includes an address tag and corresponding data;

wherein said cache controller is configured to store a portion of each of said plurality of cache lines in each of said plurality of memory sections, and wherein said

cache controller is further configured to read a portion of a first cache line concurrently with writing a portion of a second cache line.

40. (New) The cache memory system as recited in claim 39, wherein said cache controller is configured to read the data of the first cache line concurrently with writing the address tag of the second cache line.

41. (New) The cache memory system as recited in claim 39, wherein said first cache line corresponds to a given snoop request and wherein said second cache line corresponds to a another snoop request.

42. (New) The cache memory system as recited in claim 39, wherein each of said plurality of memory sections is provided on a separate memory chip.

43. (New) The cache memory system as recited in claim 39, wherein said address tag of each cache line is included in a tag field, and wherein said tag field further stores state information indicative of a coherency state of said corresponding data.

44. (New) A computer system comprising:

a processor;

a cache controller coupled to the processor; and

a cache memory coupled to said cache controller for storing a plurality of cache lines, wherein said cache memory includes a plurality of memory sections, wherein each of said memory sections is separately addressable through separate address lines coupled to said cache controller, and wherein each cache line includes an address tag and corresponding data;

wherein said cache controller is configured to store a portion of each of said plurality of cache lines in each of said plurality of memory sections, and wherein said cache controller is further configured to read a portion of a first cache line concurrently with writing a portion of a second cache line.

45. (New) The computer system as recited in claim 44, wherein said cache controller is configured to read the data of the first cache line concurrently with writing the address tag of the second cache line.

46. (New) The computer system as recited in claim 44, wherein said first cache line corresponds to a given snoop request and wherein said second cache line corresponds to a another snoop request.

47. (New) The computer system as recited in claim 44, wherein each of said plurality of memory sections is provided on a separate memory chip.

48. (New) The computer system as recited in claim 44, wherein said address tag of each cache line is included in a tag field, and wherein said tag field further stores state information indicative of a coherency state of said corresponding data.